



QORAI CORP Reports Initial FPGA Testing Demonstrating QDOS Working Model

Early hardware tests advance Q4 Nexus from software-defined architecture toward FPGA validation

ORLANDO, Fla. — October 15, 2026— QORAI CORP announced initial FPGA testing results demonstrating progress toward a working QDOS model within the company's staged Q4 Nexus development roadmap.

The tests represent an important milestone in QORAI's software-to-hardware pathway. QDOS, the company's developer-facing environment for Q4 programs and diagnostics, is being used to help load, run, inspect, and validate selected Q4 instruction and memory behaviors as the system moves toward FPGA-based hardware testing.

Initial Test Details:

FPGA Board / Platform: AMD Kria KV260 AI Starter Kit (Zynq UltraScale+ MPSoC)

RTL Language / Framework: VHDL for Q4 processor RTL and hardware modules, integrated using AMD Vivado; C++ for the QDOS diagnostic and control application using AMD Vitis.

Test Date: October 15, 2026

Validated Modules: Q4 processor instruction execution, program-counter updates, branch handling, lane-status reporting, AXI-Lite register communication, and spatial pipeline telemetry interfaces.

QDOS Commands Demonstrated: CONNECT AXI, STATUS, SPATIAL STATUS, HWTEST, JMP, BR_B, BR_T, BR_C, TRIAD, and software reference tests.

Q4 Triads Tested: BTR, BTC, BRC, and BCC.

Memory Tests: The spatial BRAM test controller and QDOS BRAMTEST diagnostic command have been integrated into the Q4 FPGA development environment. End-to-end memory integrity validation is in progress, with further debugging focused on test completion signaling and status-register readback.

Observed Results: Initial testing demonstrates successful communication between QDOS and the KV260 FPGA through the AXI interface, along with execution of the existing validated Q4 instruction tests and software reference tests. BRAM memory integrity testing remains in progress.

QORAI has completed initial FPGA-based hardware testing of selected Q4 processor functions, with all nine defined CPU hardware test cases passing. Validated functions include:

- Q4 instruction execution, program-counter updates, and tested branch handling.
- Execution of four Q4 triads: BTR, BTC, BRC, and BCC.
- QDOS-to-FPGA register communication through AXI-Lite.
- Lane-status reporting and spatial pipeline telemetry interfaces.
- Successful FPGA synthesis, bitstream generation, programming, and hardware communication.

- **9 of 9 defined CPU hardware test cases passed**, covering selected jump, branch, and triad operations.

Spatial BRAM memory testing: The integrated `BRAMTEST` diagnostic successfully completed one full test involving **1,024 read/write comparisons across 256 addresses and four 2-bit patterns, with zero mismatches**. However, other BRAM test runs experienced intermittent timeouts or inconsistent completion status. Repeatable operation is still being investigated.

Spatial Weave validation: Hardware telemetry registers are accessible, and observed Q4 state values change with tested triad instructions. Complete three-dimensional address mapping, address uniqueness, collision-free operation, and end-to-end memory integrity have not yet been established. These results demonstrate initial digital FPGA execution of selected Q4 operations and working QDOS communication with the hardware. They do **not** yet demonstrate native four-voltage processing, complete Spatial Weave Memory validation, or improved performance or storage density compared with conventional hardware.

Next validation priorities: Stabilize BRAM testing, establish reliable three-dimensional address mapping, verify spatial memory integrity, and measure performance, storage capacity, and resource utilization.

QORAI's FPGA testing is designed to compare selected hardware behavior against the company's software golden model. The goal is to validate that Q4 state representation, instruction handling, execution flow, and Spatial Weave Memory operations can be modeled through a digital FPGA implementation. The company emphasized that this stage is not native four-voltage silicon. Instead, it represents a digital hardware validation step using encoded B/T/R/C states and FPGA logic.

"This is an important proof point for QORAI," said **Robby Joshi, Founder of QORAI CORP**. "The purpose of FPGA testing is to show that QDOS and the Q4 model are not only conceptual. They can be represented, executed, traced, and diagnosed through a staged hardware pathway."

The tests support QORAI's broader roadmap:

Software Model → QDOS → Q4-ISA → Spatial Weave Memory → FPGA Validation → Future Q4 Hardware Research

QORAI believes this staged path is essential for a credible deep-tech computing platform. By validating software behavior against FPGA execution, the company can identify design constraints, improve instruction behavior, refine memory operations, and prepare for future hardware research. The company expects additional testing to focus on Q4 triad execution, state validation, memory traversal, Spatial Weave Cell Unit behavior, trace buffers, hardware diagnostics, and performance measurement. QORAI emphasized that further testing, benchmarking, and independent validation remain necessary before making performance claims.

About QORAI CORP

QORAI CORP is an Orlando-based deep-tech computing company developing **Q4 Nexus**, a patent-pending computing platform for adaptive intelligence. The company's work includes Quad Logic computing, Spatial Weave Memory, QDOS, FPGA validation, Guardian Kernel safety concepts, and future hardware research pathways.

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Forward-Looking Statement: Statements regarding QORAI's technology roadmap, Guardian Kernel, Spatial Weave Memory, Q4 hardware research, commercialization plans, potential benefits, and industry impact are forward-looking and subject to continued research, engineering validation, testing, market adoption, regulatory review, investor financing, and business execution. No future performance result, product release, safety outcome, commercial deployment, valuation, or industry adoption is guaranteed.