



QORAI CORP Advances FPGA and RTL Design Pathway for Q4 Quad Logic System

Company moves Q4 Nexus toward digital FPGA validation using staged software-to-hardware development

ORLANDO, Fla. — August 04, 2026 — QORAI CORP announced progress on its FPGA and RTL design pathway for **Q4 Nexus**, the company's Quad Logic computing platform for adaptive intelligence.

The FPGA development pathway represents an important stage in QORAI's roadmap from software-defined architecture toward hardware validation. The company's engineering approach begins with software models, QDOS, Q4-ISA instruction concepts, and Spatial Weave Memory before moving into digital FPGA implementation.

QORAI's FPGA pathway is designed to test selected elements of the Q4 architecture using conventional digital logic. This stage is not intended to be native four-voltage silicon. Instead, it uses digital encodings such as one-hot or two-bit representations to model Q4 states in hardware.

The company's FPGA research and RTL design direction includes:

- Q4 triad instruction handling
- 64-slot decoder concepts
- Q4 register structures
- QDOS command interface
- Host bridge communication
- B/T/R/C state representation
- Four-lane execution fabric
- Lane arbiter and commit authority
- Spatial Weave BRAM memory testing
- Trace comparison against software model
- Simulation and hardware bring-up pathway

QORAI's planned FPGA execution model includes a staged loop that may include fetch, validate, decode, classify, execute, bridge, regenerate, commit, and advance operations. This structure is intended to allow the company to compare software behavior against hardware behavior during validation.

"FPGA testing is the bridge between idea and engineering reality," said **Robby Joshi, Founder of QORAI CORP**. "The goal is not to jump directly into native silicon. The goal is to prove that the software model, instruction concepts, and memory operations can be represented and tested through a hardware pathway."

QORAI expects FPGA testing to help validate the Q4 execution model, QDOS interaction, triad instruction handling, and Spatial Weave Memory behavior. The company also expects FPGA work to help identify engineering constraints before any future mixed-signal, multi-voltage, or native silicon research is pursued.

The company emphasized that all hardware claims remain subject to testing, benchmarking, and independent validation. QORAI's approach is intentionally staged so that each technical layer can be evaluated before moving to the next.

QORAI CORP — Software First. FPGA Validation Next. Future Hardware Beyond That.

About QORAI CORP

QORAI CORP is an Orlando-based deep-tech computing company developing **Q4 Nexus**, a patent-pending computing platform for adaptive intelligence. The company's work includes Quad Logic computing, Spatial Weave Memory, QDOS, FPGA validation, Guardian Kernel safety concepts, and future hardware research pathways.

QORAI CORP — The Future of Computing

Media / Investor Contact:

QORAI CORP

Orlando, Florida

Email: info@qoraicorp.com

Website: www.qoraicorp.com

Forward-Looking Statement: Statements regarding QORAI's technology roadmap, Guardian Kernel, Spatial Weave Memory, Q4 hardware research, commercialization plans, potential benefits, and industry impact are forward-looking and subject to continued research, engineering validation, testing, market adoption, regulatory review, investor financing, and business execution. No future performance result, product release, safety outcome, commercial deployment, valuation, or industry adoption is guaranteed.